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gpuPOM1.0: a GPU-based Princeton Ocean Model

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Abstract. Rapid advances in the performance of the graphics processing unit (GPU) have made the GPU a compelling solution for a series of scientific applications. However, most existing GPU acceleration works for climate models are doing partial code porting for certain hot spots, and can only achieve limited speedup for the entire model. In this work, we take the mpiPOM (a parallel version of the Princeton Ocean Model) as our starting point, design and implement a GPU-based Princeton Ocean Model. We carefully considering the architectural features of the state-of-the-art GPU devices, we rewrite all mpiPOM model from the original Fortran version to the new Compute Unified Device Architecture C (CUDA-C) version. We take several accelerating methods to further improve the performance of gpuPOM, including optimizing memory access in a single GPU, overlapping communication and boundary operations among multiple GPUs, and overlapping input/output (I/O) between the hybrid Central Processing Unit (CPU) and the GPU. Our experimental results indicate that the performance of the gpuPOM on a workstation containing 4 GPUs is comparable to a powerful cluster with 408 CPU cores and it reduces the energy consumption by 6.8 times.

1 Introduction

High-resolution atmospheric, oceanic and/or climate modeling remains a significant scientific and engineering challenge because of the enormous computing, communication, and storage requirements. With the rapid development of computer architecture, in particular multi-core and many-core techniques, the computing power that can be applied to scientific problems has increased exponentially in recent decades. Some parallel computing techniques, such as the Message Passing Interface (MPI, Gropp et al. (1999)) and Open Multi-Processing (OpenMP, Chapman et al. (2008)) have been widely used to support the parallelization of numerous climate models. Moreover, as modern massive supercomputers become more and more heterogeneous because of the increasing number of different accelerating devices such as the GPU, the Intel many integrated core (Intel MIC) and reconfigurable

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Starting a name with lower case usually looks wrong because of the convention that names and the first letter of a sentence or title always start with a capital letter. It is up to you but I would suggest something like POM.gpu or POM.gpu-v1.0 when the version number also needs to be included.

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1 Introduction

High-resolution atmospheric, oceanic and ~~...~~ climate modeling remain a significant scientific and engineering challenge because of the enormous computing, communication, and storage requirements. With the rapid development of computer architecture, in particular ~~...~~lti-core and many-core ~~techniques,~~ computing power that can be applied to scientific problems has increased exponentially in recent decades. ~~...~~he parallel computing ~~techniques,~~ ~~...~~h as the Message Passing Interface (MPI, Gropp et al. (1999)) and Open Multi-Processing (OpenMP, Chapman et al. (2008)) have been widely used to support the parallelization of ~~numerous~~ climate models. ~~Moreover, modern massive~~ supercomputers become more and more heterogeneous ~~because of the increasing number of different accelerating~~ devices such as the GPU, ~~the~~ Intel ~~many integrated core~~ (Intel MIC) and reconfigurable

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Many Integrated Core

~~mputing based on~~ field programmable gate array (FPGA), new approaches are required to ~~more~~ effectively utilize the ~~emerging novel architecture, communication and input/output (I/O) to achieve order-of-magnitude acceleration required for climate models~~.

~~C~~ent years, a number of scientific codes have been ported to the GPU. Different levels of speedup were achieved for climate models using GPUs. Michalakes and Vachharajani (2008) accelerated a computationally intensive microphysics process of the Weather Research and Forecast (WRF) model with a speedup of nearly 25x; but the entire WRF model is sped up by only 1.23x. Shimokawabe et al. (2010) fully accelerated the ASUCA model – a non-hydrostatic weather model – on 528 Nvidia Tesla GT200 GPUs and achieved a speedup of 80x. Linford et al. (2009) accelerated a computationally intensive chemical kinetics kernel from the WRF model with Chemistry on an Nvidia Tesla C1060 and achieved a speedup of 8x. Leutwyler et al. (2014) accelerated a full huge operational weather forecasting model COSMO and achieved 2.8X speedup for its dynamic core. Carpenter et al. (2013) accelerated the spectral element dynamical core of the Community Earth System Model (CESM) using the GPU by 3x. Govett et al. (2010) ported the dynamics portion of the Non-hydrostatic Icosahedral (NIM) model to the GPU and achieved a speedup of 34x.Zhenya et al. (2010) adopted OpenACC Application Programming Interface (OpenACC API), which used simple compiler directives to accelerate some hot-spot functions, to accelerate the parallel ocean prog POP) by 2.2x.

Most existing GPU acceleration projects for climate models are only working on certai ots of the program, leaving a significant part of the program still running on CPUs. Therefore, there are usually frequent data exchange between CPUs and GPUs, which significantly reduces the overall performance.

The objective of our study is to shorten the high computation time of high-resolution ocean models by parallelizing their existing model structures using the GPU. Taking the para rsion of the Princeton Ocean Model (mpiPOM) ~~as an example,~~ we demonstrate how to ~~parallelize~~ ocean model to make it run efficiently on a GPU architecture. ~~Using the state-of-the-art GPU architecture, we~~ t convert the mpiPOM from its original Fortran version into a new Compute Unified Device Architecture C (CUDA-C) version. CUDA-C is the dominant programming language for GPUs. ~~We call the new version gpuPOM1.0. Then, we design and i lement several optimizing methods: (i) computation optimization in a single GPU; (ii) communication optimization among multiple GPUs, and (iii) I/O optimization between a hybrid GPU and CPU.~~

~~In terms of computing,~~ concentrate on memory access optimization ~~and~~ king better use of caches in GPU memory hierarchy. ~~We improve memory usage by~~ ng read-only data cache, local memory blocking, loop fusion, function fusion and ~~t disables~~ error-correcting code memory ~~(Error Checking & Correction, ECC memory)~~. The ~~experimental~~ ults demonstrate that ~~high memory access optimization can achieve a speedup of approximately 100x when comparing~~ a single GPU ~~against~~ ingle CPU core.

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new hardware

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This paragraph is confusing. Really it is a list of projects and speed ups which could have been placed in a table. What is missing is some sort of educated commentary - i.e. the spped of A improved by a factor of 34 because ... whereas only improved by a factor of 3 because ... .

The paragraph needs rewriting.

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This sentence repeats what was said only a few lines before.

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It does not necessarily follow. If only a few parts of the model have been converted the time taken will be almost certainly dominated by the time taken to complete the non GPU code - not the time taken to transfer data to the GPUs.

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The study is not shortening the time taken by ocean models - it is doing so only for one model.

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The MPI code has already been parallized. You need another term.

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We then optimise the code on each of the GPUs, the communications between GPUs, and between GPUs and the underlying main computer.

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by

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test

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can run the model almost a hundred times faster than a

In terms of communication, we [1]concentrate on the overlapping between the inner region computation and the outer region communication and update. With the GPUDirect communication technology, multiple GPUs in one node can communicate directly and [4]bypass the CPU. [3]In addition, with the [2] fine-grained control of the CUDA streams and its priority, inner region computation can be executed concurrently with outer region communication and updating.

In terms of I/O, we choose to split the MPI communicator into computation and I/O processes. One individual computation process and one individual I/O process are attached to one GPU. The computation process is responsible for launching kernels on the GPU and the I/O process is responsible for data copy back from the GPU and to write on disk. The computing process and the I/O process execute concurrently.

To understand the accuracy, performance and scalability of the gpuPOM, [6]we build a customized workstation with four [8]GPU 20X [9]devices inside. The [7]experimental results show that the performance of the gpuPOM running on this workstation is comparable to [11]a powerful cluster with 408 CPU cores.

The paper is organized as follows. In Section 2, we review the mpiPOM model. In Section 4, we present detailed techniques about computation optimization in a single GPU, communication optimization among multiple GPUs, and I/O optimization between a hybrid GPU and CPU. We [12]provide the corresponding experimental [13]results about [14]correctness, performance and scalability in [15]Section 5 and conclude our work in Section 7.

2 The mpiPOM

The mpiPOM is a parallel version of the Princeton Ocean Model (POM) [16]that is based on MPI. It retains most of the physics [17]package of the original POM (Blumberg and Mellor, 1983, 1987; Oey et al., 1985a, b, c; Oey and Chen, 1992a, b), [20]includes [19]also satellite and drifter assimilation schemes from the Princeton Regional Ocean Forecast System (Oey, 2005; Lin et al., 2006; Yin and Oey, 2007), [22]as well as more recently advanced features such as wind-wave induced Stokes drift, wave-enhanced mixing and Localized Ensemble Transform Kalman Filter (Oey et al., 2013; Xu et al., 2013). The POM code was reorganized and MPI was implemented by Jordi and Wang (2012) using a two-dimensional data decomposition of the horizontal domain with a halo of ghost cells. The POM is a powerful ocean model that has been used in a wide range of applications: circulation and mixing processes in rivers, estuaries, shelf and slope, lakes, semi-enclosed seas and open and global oceans. It is also at the core of various real-time ocean and hurricane forecasting systems, for examples: Japan coastal ocean and Kuroshio (Isobe et al., 2012); Adiratic Sea Forecasting System (Zavatarelli and Pinardi, 2003); the Mediterranean Sea forecasting system (Korres et al., 2007); the GFDL Hurricane Prediction system (Kurihara et al., 1995, 1998), the US' Hurricane Forecasting System (Gopalakrishnan et al., 2010, 2011) and the Advanced Taiwan Ocean Prediction system

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overlap the sending of boundary data between GPUs with the main computation.

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Data isalso sent directly between GPUs to

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Paragraph needs improving.

You need to define what you mean by MPI communicator and what you mean by computation and I/O processes.

It is also not clear wether the processes runs on the main CPU or within the GPU.

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code

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Stokes drift is another name for the wind-wave induced drift

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(Oey et al., 2013). Additionally, the model has been used to study various geophysical fluid dynamical processes (e.g. Allen and Newberger, 1996; Newberger and Allen, 2007a, b; Kagimoto and Yamagata, 1997; Guo et al., 2006; Oey et al., 2003; Zavatarelli and Mellor, 1995; Ezer and Mellor, 1992; Oey, 2005; Xu and Oey, 2011. For a more complete list please visit the POM website (http://www.ccpo.odu.edu/POMWEB).

The mpiPOM experiment that is used in this paper is one of the two designed and tested by Professor Oey and students; the codes and results are freely available at the FTP site (ftp://profs.princeton.edu/leo/mpipom/atop/tests/). The reader can see Chapter 3 of the Lecture Notes (Oey, 2014) for more detail. The test case is a dam-break problem in which warm and cold waters are initially separated in the middle of a zonally periodic channel $200km \times 50km \times 50m$ on an f-plane, with walls at the northern and southern boundaries. Geostrophic adjustment then ensues and baroclinic instability waves amplify and develop into finite-amplitude eddies in 10$\sim$20 days. The horizontal grid sizes are 1 km and there are 50 vertical sigma levels. Although the problem is a test case, the code is the full mpiPOM version that is used in the ATOP forecasting system.

The model solves the primitive equation under hydrostatic and boussinesq approximations. In the horizontal, spatial derivatives are computed either using centered-space differencing or Smolarkiewicz's positive definite advection transport algorithm (Smolarkiewicz, 1984) on a staggered Arakawa C-grid; both schemes have been tested, but the latter is reported here. In the vertical, the mpiPOM supports terrain-following sigma coordinates and a fourth-order scheme option to reduce the internal pressure-gradient errors (Berntsen and Oey, 2010). The mpiPOM uses the time-splitting technique to separate the vertically integrated equations (external mode) from the vertical structure equations (internal mode). The external mode calculation is responsible for updating surface elevation and the vertically averaged velocities. The internal mode calculation results in updates for velocity, temperature and salinity, as well as the turbulence quantities. The three-dimensional internal mode and the two-dimensional external mode are both integrated explicitly using a second-order leapfrog scheme. These two modules are the most computationally intensive kernels of the mpiPOM model.

3 GPU programming model overview

In this section, we describe the basic GPU architecture ~~in~~ programmer's perspective and ~~focus on~~ ~~how to harness the power of the~~ GPU with NVIDIA's Compute Unified Device Architecture(CUDA), ~~a programming model and computing platform that makes GPU program elegant and simple~~.

~~In the~~ GPU ~~hardware design, there are numerous~~ stream multiprocessors (SMs) ~~grouped by large numbers of CUDA cores. For an example, the~~ Nvidia's K20X GPU ~~used has~~ 14 SMs and each SM has 192 CUDA ~~cores for~~ single precision ~~operation. The~~ K20X GPU ~~can achieve~~ 3.93TFlops ~~theoretical peak performance~~ for single-precision floating point and 250GB/s ~~memory bandwidth~~.

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This section needs to be improved - remembering that this is not a computer specialist magazine. It could probably do with a diagram

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. These are SIMD (Single Instruction Multiple Data) processors containing a large number of simple CPU units.

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We carried out the conversion using four

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Each GPU contained

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processors and ??? additional processors for ... .

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The theoretical peak peformance of each

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operations if all processors are fully utilised.

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(New paragraph?) each pair of GPUs share ?? GBytes of memory, the interface hacing a potential bandwidth of

Figure 2 illustrates the memory hierarchy of K20X GPU. Each SM has its own execution units (CUDA cores, load/store units, special function units), warp-schedulers, and v on-chip faster memories such as registers, L1 cache/shared memory and texture cache. Various on-chip caches provides more opportunities to implement memory optimizations ~~on GPU platform~~. Each SM owns 64K 32 bit registers v are the fastest memory in the GPU memory hierarchy. The shared memory and the L1 cache share a 64KB ~~on-chip fast memory~~ and can be ~~configured with artificial options such as~~ 16/48KB, 32/32KB or 48/16 KB. In addition, there ~~are~~ 48 KB read-only data cache which ~~add the feature for read-only data in global memory to be loaded through the same cache.~~

There are three ~~common~~ methods ~~to port~~ program ~~from CPU~~ to GPU. The first ~~method~~ uses drop-in libraries provided by CUDA to replace the existing code, ~~such as the work implemented by~~ Siewertsen et al. (2012). The second method uses ~~simple~~ OpenACC directive as hints in the original CPU ~~code, such as the work implemented by~~ enya et al. (2010). The last method, is the most complex but the most effective, rewrites the whole program with CUDA subroutines.

In CUDA, a **kernel** is a subroutine running on the GPU. ~~Each kernel consists of a large number of threads and the~~ threads are grouped into equal size blocks which can be executed independently. Each thread block is further divided into warps, which consist of 32 consecutive threads. Threads in a warp execute the same instruction simultaneously and can be scheduled as a whole unit. Kernel function and data transfer commands in CUDA ~~has~~ optional parameter "stream ID". If "stream ID" is ~~declared~~, commands belonging different streams can be executed concurrently. It is usually used to alleviate the kernel launch overhead of subsequent independent kernels.

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4 Full GPU acceleration of the mpiPOM

Figure 1 ~~illustrates the~~ flowchart ~~of the~~ gpuPOM. The main difference between mpiPOM and gpuPOM is that the CPU in gpuPOM is only responsible for the initializing work and the outputting work. The gpuPOM begins with initializing the relevant arrays on the CPU host and then copies data from the CPU host to the GPU. The GPU does all the computations, ~~including the external mode, the internal~~

Page: 5

Number: 1 Author: djw Subject: Sticky Note Date: 30/06/2015 09:44:25
Having started to talk about the memory heirarchy - which is really about moving data efficiently - you start talking about specialised hardware. This should go in the hardware description section and you should make sure everything is defined - i.e. CUDA cores, special function usints, warp-schedulers, texture -cache. Many of these terms do no appear in other descriptions of the K20X usint.

Number: 2 Author: djw Subject: Sticky Note Date: 30/06/2015 09:44:57
Too vague for a scientific paper.

Number: 3 Author: djw Subject: Cross-Out Date: 30/06/2015 09:45:14

Number: 4 Author: djw Subject: Cross-Out Date: 30/06/2015 09:45:36

Number: 5 Author: djw Subject: Sticky Note Date: 30/06/2015 09:47:28
Use of 'share' twice with different meanings. Try to prevent this.

Number: 6 Author: djw Subject: Cross-Out Date: 30/06/2015 09:46:07

Number: 7 Author: djw Subject: Replacement Text Date: 30/06/2015 09:48:27
which

Number: 8 Author: djw Subject: Replacement Text Date: 30/06/2015 09:49:02
partitioned as

Number: 9 Author: djw Subject: Replacement Text Date: 30/06/2015 09:49:24
is a

Number: 10 Author: djw Subject: Replacement Text Date: 30/06/2015 09:53:25
is useful for holding frequently used values which remain unchanged during each stage of the processing.

Number: 11 Author: djw Subject: Cross-Out Date: 30/06/2015 09:54:29

Number: 12 Author: djw Subject: Cross-Out Date: 30/06/2015 09:54:39

Number: 13 Author: djw Subject: Replacement Text Date: 30/06/2015 09:54:12
widely used

Number: 14 Author: djw Subject: Replacement Text Date: 30/06/2015 09:54:20
for porting

Number: 15 Author: djw Subject: Inserted Text Date: 30/06/2015 09:54:34
s

Number: 16 Author: djw Subject: Replacement Text Date: 30/06/2015 09:55:05
as in

Number: 17 Author: djw Subject: Cross-Out Date: 30/06/2015 09:55:14

Number: 18 Author: djw Subject: Cross-Out Date: 30/06/2015 09:55:55

Number: 19 Author: djw Subject: Replacement Text Date: 30/06/2015 09:55:43
code. An example is

Number: 20 Author: djw Subject: Inserted Text Date: 30/06/2015 09:56:10
low level

Number: 21 Author: djw Subject: Sticky Note Date: 01/07/2015 08:53:41
Arn't your 'equal size blocks' the same as the warps you refer to in the next sentence?

Number: 22 Author: djw Subject: Inserted Text Date: 01/07/2015 08:37:14
terminology

Number: 23 Author: djw Subject: Inserted Text Date: 01/07/2015 08:37:40
single section of code or

Number: 24 Author: djw Subject: Sticky Note Date: 01/07/2015 08:54:20
Up to 32 threads?

Number: 25 Author: djw Subject: Replacement Text Date: 01/07/2015 08:52:14
The GPU is a SIMD machine, so the underlying model code is split into a series of threads each of which contains the same instructions but which operates on a separate region of the model. T

Number: 26 Author: djw Subject: Sticky Note Date: 01/07/2015 08:57:16
What is a 'Kernal function'? (or 'Kernal function command' - it is not clear what is meant).

Number: 27 Author: djw Subject: Replacement Text Date: 01/07/2015 08:57:42
both have

Comments from page 5 continued on next page

Figure 2 illustrates the memory hierarchy of K20X GPU. Each SM has its own execution units (CUDA cores, load/store units, special function units), warp-schedulers, and various on-chip faster memories such as registers, L1 cache/shared memory and texture cache. Various on-chip caches provides more opportunities to implement memory optimizations on GPU platform. Each SM owns 64K 32 bit registers which are the fastest memory in the GPU memory hierarchy. The shared memory and the L1 cache share a 64KB on-chip fast memory and can be configured with artificial options such as 16/48KB, 32/32KB or 48/16 KB. In addition, there are 48 KB read-only data cache which add the feature for read-only data in global memory to be loaded through the same cache.

There are three common methods to port a program from CPU to GPU. The first method uses drop-in libraries provided by CUDA to replace the existing code, such as the work implemented by Siewertsen et al. (2012). The second method uses simple OpenACC directive as hints in the original CPU code, such as the work implemented by Zhenya et al. (2010). The last method, is the most complex but the most effective, rewrites the whole program with CUDA subroutines.

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Number: 28 Author: djw Subject: Sticky Note Date: 01/07/2015 09:00:50
It is not clear how this might reduce the launch overhead - documentation I have seen indicates that it is used so that the GPU units can continue processing one stream of instructions while waiting for data required by another stream.

Number: 29 Author: djw Subject: Replacement Text Date: 01/07/2015 08:57:50
set

Number: 30 Author: djw Subject: Cross-Out Date: 01/07/2015 09:03:27

Number: 31 Author: djw Subject: Cross-Out Date: 01/07/2015 09:02:50

Number: 32 Author: djw Subject: Replacement Text Date: 01/07/2015 09:03:23
compilers are available for

Number: 33 Author: djw Subject: Cross-Out Date: 01/07/2015 09:03:36

Number: 34 Author: djw Subject: Cross-Out Date: 01/07/2015 09:04:32

Number: 35 Author: djw Subject: Replacement Text Date: 01/07/2015 09:04:13
would involve

Number: 36 Author: djw Subject: Replacement Text Date: 01/07/2015 09:04:19
of

Number: 37 Author: djw Subject: Replacement Text Date: 01/07/2015 09:04:50
for converting

Number: 38 Author: djw Subject: Cross-Out Date: 01/07/2015 09:05:17

Number: 39 Author: djw Subject: Inserted Text Date: 01/07/2015 09:05:27
,

Number: 40 Author: djw Subject: Cross-Out Date: 01/07/2015 09:05:42

Number: 41 Author: djw Subject: Replacement Text Date: 01/07/2015 09:05:58
did

Number: 42 Author: djw Subject: Cross-Out Date: 01/07/2015 09:06:57

Number: 43 Author: djw Subject: Cross-Out Date: 01/07/2015 09:06:04

Number: 44 Author: djw Subject: Replacement Text Date: 01/07/2015 09:06:29
for some of the

Number: 45 Author: djw Subject: Replacement Text Date: 01/07/2015 09:07:38
by

Number: 46 Author: djw Subject: Replacement Text Date: 01/07/2015 09:08:43
of optimising

Number: 47 Author: djw Subject: Cross-Out Date: 01/07/2015 09:09:55

Number: 48 Author: djw Subject: Replacement Text Date: 01/07/2015 09:09:30
is a

Number: 49 Author: djw Subject: Inserted Text Date: 01/07/2015 09:09:52
illustrating the structure

Number: 50 Author: djw Subject: Cross-Out Date: 01/07/2015 09:14:16

Number: 51 Author: djw Subject: Inserted Text Date: 01/07/2015 09:14:04
then

Number: 52 Author: djw Subject: Inserted Text Date: 01/07/2015 09:14:25
model

mode, and their interactions. In the 2D external mode loop, the depth averaged velocity UA, VA and sea surface height are calculated. In the 3D internal model loop, the fields such as velocities (U,V), temperature (T), salinity (S), and various turbulence variables are time stepped forward. Outputs such as velocity and sea surface height, are copied back to the CPU host and then written to disk at a user-specified time interval.

In our implementation, the 3D arrays of variables are stored sequentially in the order of x, y, z and the 2D arrays are stored in the order of x, y, which is the same as the original code. The vertical diffusion is solved by the tridiagonal solver (the Thomas Algorithm) which is calculated sequentially in the z direction. For simplicity, the grid is divided along x and y directions (2D block decomposition) in all kernel functions. Each GPU thread specifies a (x,y) point in the horizontal direction and performs all the calculations from surface to bottom. The thread blocks are divided into $(32,4)$. In the x direction, the block number should be a multiple of 32 threads to perform coalesced memory access within a warp. In the y direction, we tested many thread numbers, such as 4 and 8, and obtained similar performances. We finally choose 4 because we attempt to obtain more blocks to distribute the workload among stream multiprocessors (SM) more uniformly and also to obtain enough occupancy (Volkov, 2010). Occupancy is the percentage of threads active per multiprocessor.

In the following sections, we introduce the general optimizations of the gpuPOM in GPU and the special optimizations of the gpuPOM following the state-of-the-art GPU architecture. Then, we present the design of communications for various processes and multiple GPUs within a node. Finally, we describe the design of I/O overlapping for hybrid CPU and GPU architecture.

4.1 Computational optimizations in a single GPU

Managing the significant performance difference between off-chip and on-chip memory is the primary concern of a GPU programmer. As shown on the right side of Fig. 2, we propose five key optimizations to fully utilize the faster on-chip memory of the GPU and describe the relationships between the GPU memory hierarchy and each optimization in the following.

(A) Read-only data cache utilization. Effective use of the new 48KB directly-access and read-only data cache in the K20X GPU can improve the performance of memory intensive kernels. This feature will be automatically enabled and utilized as long as certain conditions are met. We add "const __restrict__" qualifiers to the parameter pointers in gpuPOM to explicitly allocate the read-only data cache for our program. The "LDG.E" instruction will then appear in the disassembling code, and Nvidia Visual Profiler(NVVP) software will show that the read-only data cache is actually being utilized.

As an example, consider the calculations of advection and the horizontal diffusion terms. Because mpiPOM adopts the Arakawa C-grid, the update of $T(i,j,k)$ requires the value of $u(i,j,k)$, $u(i+1,j,k)$, $v(i,j,k)$ and $v(i,j+1,k)$, in addition to the value of horizontal kinematic viscosity, aam, from four neighboring grid points. In one time step, the arrays of u and v must be accessed twice,

Page: 6

Number: 1 Author: djw Subject: Cross-Out Date: 01/07/2015 09:14:16

Number: 2 Author: djw Subject: Sticky Note Date: 01/07/2015 09:15:18
Copied back by the GPU or CPU?

Number: 3 Author: djw Subject: Sticky Note Date: 01/07/2015 09:15:46
by the CPU?

Number: 4 Author: djw Subject: Inserted Text Date: 01/07/2015 09:16:32
, as in the original code

Number: 5 Author: djw Subject: Cross-Out Date: 01/07/2015 09:16:44

Number: 6 Author: djw Subject: Cross-Out Date: 01/07/2015 09:16:50

Number: 7 Author: djw Subject: Cross-Out Date: 01/07/2015 09:17:45

Number: 8 Author: djw Subject: Inserted Text Date: 01/07/2015 09:17:20
V

Number: 9 Author: djw Subject: Replacement Text Date: 01/07/2015 09:17:38
using a

Number: 10 Author: djw Subject: Inserted Text Date: 01/07/2015 09:19:01
in our kernel functions

Number: 11 Author: djw Subject: Sticky Note Date: 01/07/2015 09:21:09
In the x and y directions?

Number: 12 Author: djw Subject: Inserted Text Date: 01/07/2015 09:20:23
then

Number: 13 Author: djw Subject: Sticky Note Date: 01/07/2015 09:23:27
coalesced memory access needs to be defined for a non-computer specialist readership.

Number: 14 Author: djw Subject: Replacement Text Date: 01/07/2015 09:22:11
needs to

Number: 15 Author: djw Subject: Replacement Text Date: 01/07/2015 09:24:51
this produced

Number: 16 Author: djw Subject: Inserted Text Date: 01/07/2015 09:25:00
and allowed us to

Number: 17 Author: djw Subject: Cross-Out Date: 01/07/2015 09:25:47

Number: 18 Author: djw Subject: Replacement Text Date: 01/07/2015 09:25:27
more unifirmly amongst the

Number: 19 Author: djw Subject: Replacement Text Date: 01/07/2015 09:28:18
. It also increased the occupancy, the average number of active threads in each multiprocessor

Number: 20 Author: djw Subject: Cross-Out Date: 01/07/2015 09:28:23

Number: 21 Author: djw Subject: Cross-Out Date: 01/07/2015 09:32:15

Number: 22 Author: djw Subject: Sticky Note Date: 01/07/2015 09:34:15
Have I got this right - are you talking about special improvements for the X??? independent of the GPU to GPU connections discussed next?

Number: 23 Author: djw Subject: Replacement Text Date: 01/07/2015 09:32:21
for

Number: 24 Author: djw Subject: Sticky Note Date: 01/07/2015 10:31:28
Later I could not find an example of special optimizing. Possibly your two classes here are:
1. Loop unrolling/fusion etc - standard computer improvements.
2. Optimizations special to the GPU
If so make it clearer here and split section 4.1 in the same way.

Number: 25 Author: djw Subject: Replacement Text Date: 01/07/2015 09:32:45
some

Number: 26 Author: djw Subject: Replacement Text Date: 01/07/2015 09:32:59
for current

Number: 27 Author: djw Subject: Sticky Note Date: 01/07/2015 09:35:30

Comments from page 6 continued on next page

mode, and their interactions. In the 2D external mode loop, the depth averaged velocity UA, VA and sea surface height are calculated. In the 3D internal model loop, the fields such as velocities (U,V), temperature (T), salinity (S), and various turbulence variables are time-stepped forward. Outputs such as velocity and sea surface height, are copied back to the CPU host and then written to disk at a user-specified time interval.

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Should this be 'have implemented'?

Number: 28 Author: djw Subject: Sticky Note Date: 01/07/2015 09:34:45
Why?

Number: 29 Author: djw Subject: Replacement Text Date: 01/07/2015 09:36:05
better

Number: 30 Author: djw Subject: Replacement Text Date: 01/07/2015 09:40:20
fast

Number: 31 Author: djw Subject: Inserted Text Date: 01/07/2015 09:40:55
. We

Number: 32 Author: djw Subject: Sticky Note Date: 01/07/2015 09:43:37
It might be cleaner to say something like: We describe how each optimisation makes use of the GPU memory structure in the following.

Number: 33 Author: djw Subject: Sticky Note Date: 01/07/2015 09:45:52
What conditions?

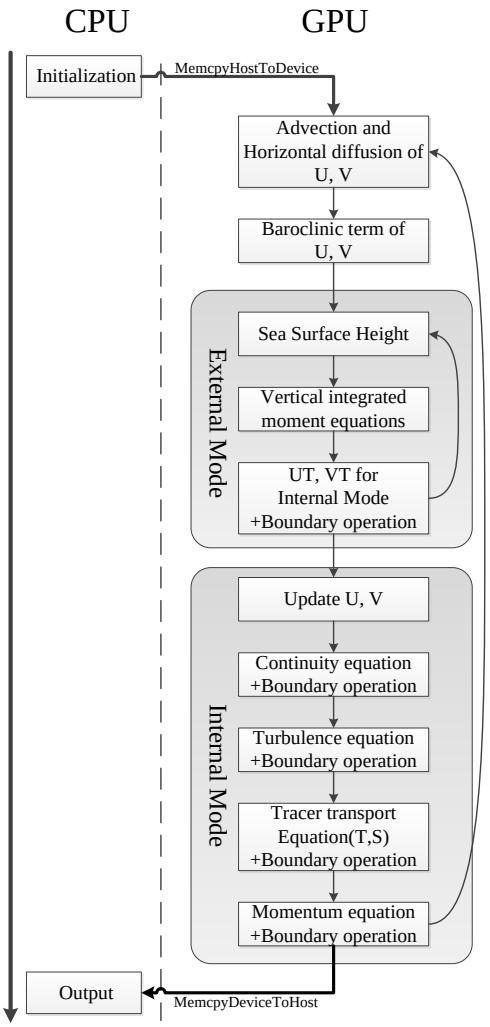

Figure 1. gpuPOM flowchart

and the aam array must be accessed four times. Therefore it is natural to use the read-only data cache to improve the data locality of gpuPOM. This optimization improves the performance of this part by 18.8%.

(B) Local memory blocking. Cache blocking is a common method to improve data reuse in parallel computing. In this method, a small subset of a dataset is loaded into the on-chip faster memory (e.g., the L1/L2 cache in the GPU and the CPU) and then the small data block is repeatedly accessed by the program. It is helpful to reduce the need to access the off-chip with high latency memory (e.g., global memory on the GPU). Because regular global memory access cannot be cached

This page contains no comments

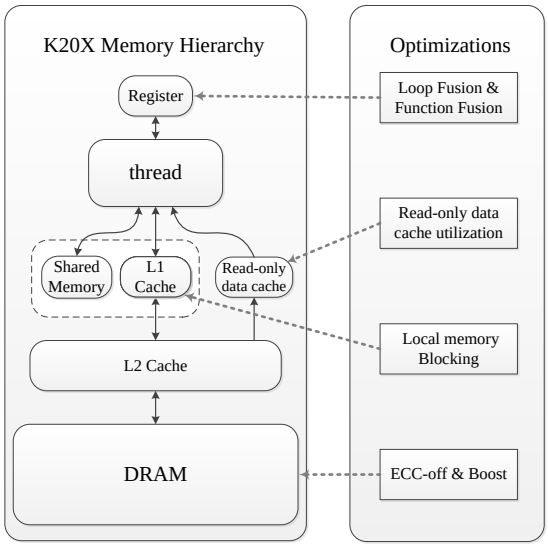

Figure 2. The memory hierarchy of K20X GPU and the relationships with each optimizations

in L1 cache for K20X GPU, the method used here is to pull the data from local memory to the L1 cache.

For the subroutines about vertical diffusion and source/sink terms, the chasing method is used to solve a tridiagonal matrix along the vertical direction for each grid point individually. As shown in Algorithm 1, the 3D temporary arrays in the original code, such as ee, gg, that store row transformation coefficients are streamed from memory. However, these arrays are too large to reside in the cache entirely; code efficiency is therefore decreased. We find th[1]n thread performs a column calculation from surface to bottom and there is no communication. Thus, we declare 1D arrays ee_new, gg_new in local memory to replace the original 3D global arrays. Their size is equal to the level of ocean, $nz-1$, which is typically a very small value.

In the chasing method, these local arrays are accessed twice within one thread, one from $k=0$ to $k=nz-1$ and another from $k=nz-1$ to $k=0$. After blocking the vertical direction arrays in local memory, L1 cache is fully utilized although some of them may be spilled to global memory. The performance of the subroutines about vertical diffusion and source/sink terms is improved by 35.3% when using the local memory blocking technique.

(C) Loop fusion. Loop fusion is an effective method to store scalar variables in registers for data[2] reuse. Registers are the fastest memory in the GPU memory hierarchy. For example, as shown in Algorithm 2, if the variable *drhox(k, j, i)* must be read several times in multiple loops, we can fuse these loops into one. Therefore, the *drhox(k, j, i)* will be read from the global memory the first

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Number: 1 Author: djw Subject: Sticky Note Date: 01/07/2015 09:47:49
Communication between what?

Number: 2 Author: djw Subject: Sticky Note Date: 01/07/2015 09:50:14
This is not a GPU optimisation - it is a standard scheme used in many models. Maybe you should describe it separately as a basic optimisation of the POM model applicable to any type of cache based computer.

Algorithm 1 A simple example of local memory blocking

```
/*********************
* Origin CUDA-C code
*********************/
//ee, gg are parameter pointers of the function
//that represent the use of global memory

for (k = 1; k < nz-2; k++){
    ee[k][j][i] = ee[k-1][j][i]*A[k][j][i];
    gg[k][j][i] = ee[k-1][j][i]*gg[k-1][j][i]-B[k][j][i];
}

for (k = nz-3; k >= 0; k++){
    uf[k][j][i] = (ee[k][j][i]*uf[k+1][j][i]+gg[k])*C[k][j][i];
}
/*******************
* After local memory blocking
*******************/
//ee_new, gg_new are 1-D array declared in function
//that represent the use of local memory

for (k = 1; k < kbm1; k++){
    ee_new[k] = ee_new[k-1]*A[k][j][i]
    gg_new[k] = ee_new[k-1]*gg_new[k-1]-B[k][j][i];
}

for (k = nz-3; k >= 0; k++){
    uf[k][j][i] = (ee_new[k]*uf[k+1][j][i]+gg_new[k])*C[k][j][i];
}
```

This page contains no comments

time and then repeatedly read from a register. This method can also be applied in a number of the mpiPOM subroutines.

Take the kernel *profq* as an example. After rewriting part of source code with loop fusion, the device memory transactions decrease by 57%, while the registers used per thread increase from 46 to 72, as reported in NVVP. Although the occupancy achieved decrease from 61.1% to 42.7%, the performance of this kernel is improved by 28.6%.

Algorithm 2 A simple example of loop fusion

```
/*********************
* Origin cuda-c code
*********************/
for (k = 1; k < kbm1; k++){
   drhox[k][j][i] = drhox[k-1][j][i] + A[k][j][i];
}

for (k = 0; k < kbm1; k++){
   drhox[k][j][i] = drhox[k][j][i] * B[k][j][i];
}

/*********************
* After loop fusion
*********************/
for (k = 1; k < kbm1; k++){
   drhox[k][j][i] = drhox[k-1][j][i] + A[k][j][i];
   drhox[k-1][j][i] = drhox[k-1][j][i] * B[k][j][i];
}
drhox[0][j][i] = drhox[0][j][i] + B[k][j][i];
```

(D) Function fusion. Because we can fuse the loops in which the same arrays are accessed, we can also fuse functions in which similar formulas are calculated and the same arrays are accessed. For example, the $advv$ and $advu$ functions of the mpiPOM calculate advection in longitude and latitude, respectively, and they can be fused into one subroutine. This optimization benefits from the elimination of the redundancy calculations.

This optimization is also useful for the situation in which one function is called several times to calculate different tracers. For example, the $proft$ functions of the mpiPOM is called twice – once for temperature and once for salinity. Their computing formulas are similar and certain common arrays are accessed; these functions were modified to calculate temperature and salinity simultaneously. The method of Function fusion improves the performance of these functions by 28.8%.

Number: 1 Author: djw Subject: Sticky Note Date: 01/07/2015 09:51:06
Again this is a basic optimisation applicable to any cache based CPU.

Table 1. Different subroutines adopt different optimizations in gpuPOM

Subroutines	A	B	C	D	E	Speedup
Adv & Hor diff	√		√	√	√	2.05X
Ver diff		√	√	√	√	2.82X
Baroclinic	√		√		√	2.08X
Continuity equ	√				√	1.39X
Vorticity	√		√		√	3.19X
State equ	√				√	1.35X

(E)ECC-off and GPU boost. Because ECC memory consumes some amount of memory bandwidth, we can improve the GPU global memory bandwidth by disabling the error checking and memory correcting features. Also, the memory bandwidth that can be achieved is improved by enhancing the clock of SM core. In our implementation, we overclock the default clock of K20X GPU from 732 MHz to 784 MHz. The methods of ECC-off and GPU boost improves the performance of the whole application by 13.8%.

We divide all the gpuPOM subroutines into different categories based on their different computation patterns. As shown in Table 1, in gpuPOM, we deploy different optimizations in different categories to achieve improved performance; these categories are now described.

(1)Category 1: Advection and horizontal diffusion(adv)

This category has 6 subroutines, and calculates the advection and horizontal diffusion and in the case of velocity, the pressure gradient and Coriolis terms. Here it is possible to reuse data among adjacent threads, and the subroutines therefore benefit from using read-only data cache and shared-memory. Also, the variables are calculated in different loops of one function or in different functions, so the loop fusion and function fusion optimizations apply to this part.

(2)Category 2: vertical diffusion(ver)

This category has 4 subroutines, and calculates the vertical diffusion. In this part, chasing method is used in the tridiagonal solver in the k-direction. The main feature is that data is reused twice within one thread, while data is accessed once from $k = 0$ to $k = nz-1$ and once from $k = nz-1$ to $k = 0$. The subroutines are significantly sped up after grouping the k-direction variable in local memories.

(3)Category 3: vorticity(vort), baroclinic(baro), continuity equation(cont) and equation of state(state)

This category is less time consuming than the two categories above, but it also benefits from our optimizations. Because there exists data reuse with adjacent threads, the use of read-only data cache improves efficiency. For vort, there is data reuse within one thread, and loop fusion improves the efficiency.

The main bottleneck of the mpiPOM is memory-bound problem. To confirm this issue, we use the Performance API(Browne et al., 2000) to estimate floating point operation count and the memory

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Number: 1 Author: djw Subject: Sticky Note Date: 01/07/2015 09:51:56
Again not necessarily a basic GPU optimisation.

Number: 2 Author: djw Subject: Sticky Note Date: 01/07/2015 09:52:31
Start new sub-section.

Number: 3 Author: djw Subject: Sticky Note Date: 01/07/2015 09:56:14
1. 'Memory bound' really means not enough memory. I think you mean 'memory bandwidth limited'. Needed for a non-computer specialist readership.
2. A bottleneck is a problem. Try and avoid repetition.

Number: 4 Author: djw Subject: Sticky Note Date: 01/07/2015 09:57:51
Is this an analysis of the compiled code?

Number: 5 Author: djw Subject: Inserted Text Date: 01/07/2015 09:58:23
the

access(store/load) instruction count. Results reveal that the computational intensity(flops/byte) of the mpiPOM is around 1:3.3, while the computational intensity provided by SandyBridge E5-2670 CPUs is 7.5:1. Large arrays are mostly streamed from memory and shows little locality. According to the roofline model(Williams et al., 2009), the whole mpiPOM is mainly memory-bounded. In addition, the mpiPOM suffers from a flat profiling results, with the most time-consuming subroutine just occupying 20% of the total execution time. Namely, there are no obvious hot spot functions in the mpiPOM and porting a handful of subroutines to GPU is not helpful to improve the model efficiency. That is the reason that we need to port the whole program from CPU to GPU.

To alleviate the memory bound problem, an optimization method that is frequently used is cache blocking. It is usually cache beneficial to use vertical index as the innermost array index(z,x,y ordering). For the mpiPOM with $962 \times 722 \times 51$ test case, one array has $962 \times 722 \times 4$bytes= 2.6MBytes in the x-y plane, while one CPU has a 32KB per-core L1 cache, 256KB per-core L2 cache and 20MB shared L3 caches. Take the chasing method in vertical diffusion terms as an extreme case. If x,y,z ordering is used, in terms of calculation along z-axis, each x-y plane is blocked in L3 cache for reuse. When traversing backwards along z, the data needed are all evicted. If z,x,y ordering is used, in terms of calculation along z-axis, each k column data is blocked in L1 cache for reuse. When traversing backwards along z, the data remains valid in L1 cache. Unfortunately, the mpiPOM uses east-west index as the innermost array index. However, for mpiPOM, i,k,y ordering has to be avoided to satisfy GPU memory coalescing, which is also demonstrated in Shimokawabe et al. (2010). We make east-west (x) as innermost index(x,y,z ordering). A big difference for memory optimizations between GPU and CPU is that, in GPU, programmers can artificially choose which array to store in cache. Moreover, GPU provides various on-chip caches, such as L1/L2 cache, shared memory, texture cache. Thus, according to how the arrays are used, we can put different arrays in different caches. In the gpuPOM, we have explored a better data placement on different caches for different terms, besides conventional cache blocking optimizations.

4.2 Communication optimizations among multiple GPUs

In this section, we present the optimizing strategies used ~~to harness the computing power of multiple~~ GPUs. With multiple GPUs, the computing domain is divided into smaller blocks than with a single GPU. The performance of GPU computing is faster and the memory requirement for each GPU is reduced. To utilize multiple GPUs, an effective domain decomposition method and communication method should be employed. We split the domain along the x and y directions (2-D decomposition) and assign each MPI process for one subdomain, following Jordi and Wang (2012). Then, we attach the MPI process to one GPU and send messages from one GPU to another. Shimokawabe et al. (2010) and Yang et al. (2013) proposed some fine-grained overlapping methods of GPU computation and CPU communication to improve the simulation performance. An important ~~common~~ issue is that the communications between multiple GPUs explicitly require the participation of the CPU. In our

Page: 12

Number: 1 Author: djw Subject: Sticky Note Date: 01/07/2015 10:00:20
Expand for the audience (i.e. floating point operations per byte transferred to or from memory).

Number: 2 Author: djw Subject: Sticky Note Date: 01/07/2015 10:02:18
You need a context, possibly:
"... provide by a modern high performance CPU (the Intel Sandy ...) ..."

Number: 3 Author: djw Subject: Sticky Note Date: 01/07/2015 10:03:16
For the audience - what do you mean by locality?

Number: 4 Author: djw Subject: Sticky Note Date: 01/07/2015 10:04:16
For the audience explain briefly what the roofline model is - many will not have easy access to your references.

Number: 5 Author: djw Subject: Sticky Note Date: 01/07/2015 10:04:59
Again for the audience - what does flat profiling mean?

Number: 6 Author: djw Subject: Sticky Note Date: 01/07/2015 10:06:34
Poor use of the word. Better would be - this means - or - as a result.

Number: 7 Author: djw Subject: Sticky Note Date: 01/07/2015 10:08:47
This has already been covered once. I suggest you move this discussion there to save repetition of many of your statements.

Number: 8 Author: djw Subject: Sticky Note Date: 01/07/2015 10:09:40
In POM it may be true but not with every code.

Number: 9 Author: djw Subject: Sticky Note Date: 01/07/2015 10:15:06
This needs more explanation. As L3 cache is large enough to hold the whole model I presume you mean L1 and/or L2 cache.

For the audience you also need to explain why it needs to be evicted. Maybe the work overwritten would be more accurate and better for this audience.

Number: 10 Author: djw Subject: Sticky Note Date: 01/07/2015 10:16:23
'blocked' is a specialist work. 'kept' might be better.

Number: 11 Author: djw Subject: Sticky Note Date: 01/07/2015 10:16:59
remove 'valid'? Why is it needed?

Number: 12 Author: djw Subject: Sticky Note Date: 01/07/2015 10:20:47
What is GPU memory coalescing?
Why does it need to be satisfied?

You say it is also demonstrated by Shimokawabe so
"Where have you demonstrated it here?".
What did you do?
Where are the results?

Number: 13 Author: djw Subject: Inserted Text Date: 01/07/2015 10:17:38
the

Number: 14 Author: djw Subject: Inserted Text Date: 01/07/2015 10:17:50
code

Number: 15 Author: djw Subject: Sticky Note Date: 01/07/2015 10:21:53
'make' - surely you decided to keep the basic POM ordering.

Number: 16 Author: djw Subject: Sticky Note Date: 01/07/2015 10:25:17
Do not use 'various' in a scientific paper to escape being more specific.

You have already stated that there are L1, l2 and L3. Do not repeat.

It is not obvious here what you mean by shared memory in addition to the caches.

Texture cache is new. presumably you mean the read-only cache discussed earlier.

Number: 17 Author: djw Subject: Sticky Note Date: 01/07/2015 10:26:58
This is all too long. There are lots of caches. You can optimize their use.

Anything more should be about how they are best optimized.

Number: 18 Author: djw Subject: Sticky Note Date: 01/07/2015 10:35:20
Why is it divided into smaller blocks. Is this you decision or is it an essential requirement due to some reason I have missed?

Number: 19 Author: djw Subject: Replacement Text Date: 01/07/2015 10:33:25
when coupling

Number: 20 Author: djw Subject: Sticky Note Date: 01/07/2015 10:36:27
Is this because there are smaller blocks or because more GPUs are involved?

Number: 21 Author: djw Subject: Sticky Note Date: 01/07/2015 10:37:28
What do you mean by an effective domain decomposition method. How do you measure effectiveness?

Comments from page 12 continued on next page

access(store/load) instruction count. Results reveal that the computational intensity(flops/byte) of the mpiPOM is around 1:3.3, while the computational intensity provided by SandyBridge E5-2670 CPUs is 7.5:1. large arrays are mostly streamed from memory and shows little locality. According to the roofline model(Williams et al., 2009), the whole mpiPOM is mainly memory-bounded. In addition, the mpiPOM suffers from a flat profiling results, with even the most time-consuming subroutine just occupying 20% of the total execution time. Namely, there are no obvious hot spot functions in the mpiPOM and porting a handful of subroutines to GPU is not helpful to improve the model efficiency. That is the reason that we need to port the whole program from CPU to GPU.

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4.2 Communication optimizations among multiple GPUs

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Number: 22 Author: djw Subject: Sticky Note Date: 01/07/2015 10:40:12

Up to now you have not discussed MPI at all. So some introduction is necessary. Also what do you mean here by an MPI process? Do you mean the independent code that normally runs on a separate CPU in a multi-processor CPU system.

Number: 23 Author: djw Subject: Sticky Note Date: 01/07/2015 10:47:53

How are the two parts of this sentence connected?

I think you need to be more explicit along the lines of - control of the computation within each domain and transfer of data between the GPU and main memory is handled by the MPI process but where possible transfer of data between domains is handled by the GPUs themselves.

Number: 24 Author: djw Subject: Cross-Out Date: 01/07/2015 10:48:23

Number: 25 Author: djw Subject: Inserted Text Date: 01/07/2015 10:48:36

in their work

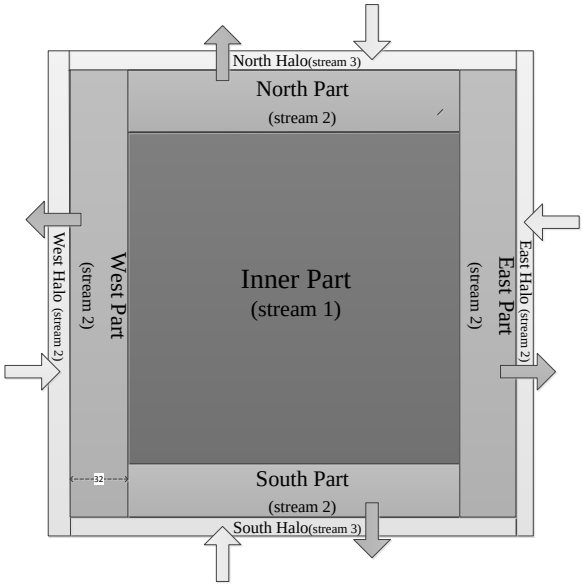

Figure 3. Data decomposition in gpuPOM

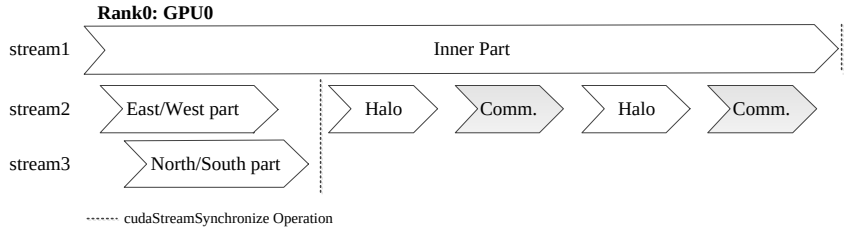

Figure 4. The workflow of multiple streams on the GPU. The “inner/east/west/north/south part" and “Halo" refer to computation and update of corresponding part. “Comm." refers to communication between processes, which implies synchronization.

work, we hope to implement the communication to bypass the CPU to fully employ the capability of the GPU.

State of the art MPI libraries, such as OpenMPI and MVAPICH2, have announced their support for MPI communication directly from GPU memory, which is known as CUDA-aware MPI. We tried MVAPICH2 to implement direct communication among multiple GPUs at first. However, we found that the boundary operation and MPI communication occupied nearly 15% of the total runtime after GPU porting.

To fully overlap the boundary operations and MPI communications with computation, we adopt the data decomposition method shown in Fig. 3. The data region is decomposed into three parts: the inner part, the outer part, and the halo part. The outer part includes east/west/north/south part, and

Page: 13

Number: 1 Author: djw Subject: Cross-Out Date: 01/07/2015 10:49:04

Number: 2 Author: djw Subject: Cross-Out Date: 01/07/2015 10:49:27

Number: 3 Author: djw Subject: Cross-Out Date: 01/07/2015 10:49:33

Number: 4 Author: djw Subject: Inserted Text Date: 01/07/2015 10:49:07
The

Number: 5 Author: djw Subject: Cross-Out Date: 01/07/2015 10:49:46

Number: 6 Author: djw Subject: Inserted Text Date: 01/07/2015 10:49:59
to main

Number: 7 Author: djw Subject: Replacement Text Date: 01/07/2015 10:50:17
. This is termed

Number: 8 Author: djw Subject: Inserted Text Date: 01/07/2015 10:50:30
using

Number: 9 Author: djw Subject: Cross-Out Date: 01/07/2015 10:50:37

Number: 10 Author: djw Subject: Cross-Out Date: 01/07/2015 10:50:47

Number: 11 Author: djw Subject: Replacement Text Date: 01/07/2015 10:50:56
but

Number: 12 Author: djw Subject: Cross-Out Date: 01/07/2015 10:52:08

Number: 13 Author: djw Subject: Replacement Text Date: 01/07/2015 10:51:50
inter-domain

Number: 14 Author: djw Subject: Inserted Text Date: 01/07/2015 10:52:00
then

Number: 15 Author: djw Subject: Sticky Note Date: 01/07/2015 10:53:43
Such a domain decomposition is fairly standard. Is something similar not done in POM?

Number: 16 Author: djw Subject: Inserted Text Date: 01/07/2015 10:52:32
Instead

Number: 17 Author: djw Subject: Sticky Note Date: 01/07/2015 10:58:15
I think it would be better to replace 'part' by 'region' in this section.

Number: 18 Author: djw Subject: Cross-Out Date: 01/07/2015 10:54:38

Number: 19 Author: djw Subject: Cross-Out Date: 01/07/2015 10:54:34

Number: 20 Author: djw Subject: Inserted Text Date: 01/07/2015 10:54:38
a

~~The halo part also includes east/west/north/south halos to exchange~~ data with neighbors. In CUDA, a stream is a sequence of commands that execute in order; different streams can also execute concurrently with different priorities. In our design, the inner part, which is the most time-consuming ~~part with the largest workload~~ is allocated to stream 1 ~~in which to execute~~. The east/west outer part is allocated to stream 2 and the north/south outer part is allocated to stream 3. In the east/west outer part, the width is set to 32 to ensure coalesced memory access in a warp ~~to improve performance~~. The halo part is also allocated to stream 2.

The workflow of multiple streams on the GPU is shown in Fig. 4. The east/west/north/south parts are normal kernel functions that can run in parallel with the inner part through different streams. The communication operations are implemented by ~~$cudaMemcpyAsync$, which is~~ an asynchronous CUDA memory copy function. The corresponding synchronization operation between the CPU and the GPU or among MPI processes are implemented with $cudaStreamSynchronize$ function and $MPI\_barrier$ function. To hide the subsequent communication by the inner part, stream 2 and stream 3 for the outer part have higher priority to preempt the computing resource from stream 1 at any time.

~~Current CUDA-aware MPI implementation such as~~ MVAPICH2 ~~is~~ not suitable for the "Communication ~~in~~ Fig. 3. We found the ~~two-sided~~ MPI functions MPI_Send and MPI_Recv will block the current stream so that the concurrency pipeline is broken. The probable cause is ~~synchronous~~ $cudaMemcpy$ function ~~is called in the current implementation of~~ MPI_Send and MPI_Recv, ~~according to~~ Potluri et al. (2012). Moreover, the implementation of non-contiguous MPI datatype for communication between GPUs is not efficient enough for the gpuPOM. The computation time of many kernels is about a few hundred microseconds to a few milliseconds while MPI latency for our message size is about the same, which means the outer part update and communication can not be fully overlapped.

From CUDA 4.1, the Inter-Process Communication (IPC) feature has been introduced to facilitate direct data copy ~~among multiple~~ GPU ~~buffers that are allocated by different processes~~. The IPC is implemented by creating and exchanging memory handles ~~among processes~~ and obtaining the device buffer pointers of others. This feature ~~has been~~ utilised in CUDA-aware MPI libraries ~~to optimise communications within a node.~~ Therefore, we decided to implement the communication among multiple GPUs by calling the low-level IPC functions and asynchronous CUDA memory copy functions directly~~, instead of using high-level CUDA-aware MPI functions~~. Our communication optimizations among multiple GPUs are mainly implemented with the following two optimizations.

First, we put the phases of creating, exchanging and opening relevant memory handles into the initialization phase of the gpuPOM, which is executed only once. This method can remove the overhead of IPC memory handle operations during each MPI communication operation. The $cudaMemcpyAsync$ function with the corresponding device buffer pointers of neighbor processes replaces the original MPI functions.

Page: 14

Number: 1 Author: djw Subject: Sticky Note Date: 01/07/2015 10:56:01
This description of a stream should go in the earlier hardware/software description sections.

Number: 2 Author: djw Subject: Cross-Out Date: 01/07/2015 10:54:34

Number: 3 Author: djw Subject: Replacement Text Date: 01/07/2015 10:54:49
which exchanges

Number: 4 Author: djw Subject: Cross-Out Date: 01/07/2015 10:56:24

Number: 5 Author: djw Subject: Cross-Out Date: 01/07/2015 10:56:34

Number: 6 Author: djw Subject: Cross-Out Date: 01/07/2015 10:57:26

Number: 7 Author: djw Subject: Sticky Note Date: 01/07/2015 11:00:34
All the halo or just east-west. If the latter remove this sentence and change previous sentences to include the halo region.

Number: 8 Author: djw Subject: Sticky Note Date: 01/07/2015 11:01:37
Do you really mean streams 2 and 3 which can run in parallel with stream 1.

Number: 9 Author: djw Subject: Sticky Note Date: 01/07/2015 11:04:47
Such detail is not needed - or, if you insist ,should be added in brackets at the end of the sentence

Number: 10 Author: djw Subject: Sticky Note Date: 01/07/2015 11:03:27
between domains

Number: 11 Author: djw Subject: Cross-Out Date: 01/07/2015 11:03:46

Number: 12 Author: djw Subject: Sticky Note Date: 01/07/2015 11:06:52
I suggest using:
a CUDA syncronisation command or function.
1 MPI barrier function

Number: 13 Author: djw Subject: Sticky Note Date: 01/07/2015 11:08:52
This implies the inner part is hiding something - which I do not think you mean. Rewrite.

Number: 14 Author: djw Subject: Sticky Note Date: 01/07/2015 11:10:31
Expand -> communication

Number: 15 Author: djw Subject: Cross-Out Date: 01/07/2015 11:10:00

Number: 16 Author: djw Subject: Sticky Note Date: 01/07/2015 11:58:11
Are these sending and receiving data to the GPU or to other MPI processes?

What is meant here by the 'current' stream. We have been told that each MPI processes has 3.

If this is to do with sending data to the GPU later we are told that kernels only involve code between MPI calls - so how can a kernal be stopped - or does your MVAPICH version of POM not do this?

Number: 17 Author: djw Subject: Replacement Text Date: 01/07/2015 11:09:55
We found that

Number: 18 Author: djw Subject: Inserted Text Date: 01/07/2015 11:10:03
was

Number: 19 Author: djw Subject: Cross-Out Date: 01/07/2015 11:52:41

Number: 20 Author: djw Subject: Replacement Text Date: 01/07/2015 11:11:01
section of

Number: 21 Author: djw Subject: Replacement Text Date: 01/07/2015 11:58:42
the

Number: 22 Author: djw Subject: Replacement Text Date: 01/07/2015 11:59:09
called by

Number: 23 Author: djw Subject: Sticky Note Date: 01/07/2015 12:01:16
What do you mean by a non-contiguous MPI datatype?
What do you mean by 'the implimitation? Whos's implimitation?
Why is it not efficient enough?

Number: 24 Author: djw Subject: Cross-Out Date: 01/07/2015 11:59:15

Comments from page 14 continued on next page

~~the halo part also includes east/west/north/south halos~~ ~~to exchange~~ data with neighbors. In CUDA, a stream is a sequence of commands that execute in order; different streams can also execute concurrently with different priorities. In our design, the inner part, which is the most time-consuming ~~part with the largest workload~~ is allocated to stream 1 ~~in which to execute~~. The east/west outer part is allocated to stream 2 and the north/south outer part is allocated to stream 3. In the east/west outer part, the width is set to 32 to ensure coalesced memory access in a warp ~~to improve performance~~. The halo part is also allocated to stream 2.

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~~Current CUDA-aware MPI implementation such as~~ MVAPICH2 ~~is~~ not suitable for the "Comm~~" part in~~ Fig. 3. We found the ~~two sided~~ MPI functions MPI_Send and MPI_Recv will block the current stream so that the concurrency pipeline is broken. The probable cause is ~~synchronous~~ $cudaMemcpy$ function ~~is called in the current implementation of~~ MPI_Send and MPI_Recv, ~~according to~~ Potluri et al. (2012). Moreover, the implementation of non-contiguous MPI datatype for communication between GPUs is not efficient enough for the gpuPOM. The computation time of many kernels is about a few hundred microseconds to a few milliseconds while MPI ~~latency~~ for our message size is about the same, which means the outer part update and communication can not be fully overlapped.

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Number: 25 Author: djw Subject: Sticky Note Date: 01/07/2015 12:08:26
The computation time of many of our kernels?
I think one problem here is that you started saying that you used direct communication between GPUs - but here without introduction you appear to be talking about transfers via the CPU.

Is this MPI latency an MPI problem due to a high CPU overhead or is it a result of a limited CPU/GPU memory bandwith.

Number: 26 Author: djw Subject: Sticky Note Date: 01/07/2015 12:09:35
Later you say that the outer part updade occurs before communication - so why is any overlap an issue?

Number: 27 Author: djw Subject: Replacement Text Date: 01/07/2015 12:11:02
between

Number: 28 Author: djw Subject: Replacement Text Date: 01/07/2015 12:10:51
s

Number: 29 Author: djw Subject: Sticky Note Date: 01/07/2015 12:12:00
others what?

Number: 30 Author: djw Subject: Cross-Out Date: 01/07/2015 12:11:32

Number: 31 Author: djw Subject: Cross-Out Date: 01/07/2015 12:13:03

Number: 32 Author: djw Subject: Sticky Note Date: 01/07/2015 12:15:19
'Therefore' does not fit. Just because MVAPICH2, which you did not like, used IPC is no good reason for dumping MVAPICH2 and then using IPC.

Number: 33 Author: djw Subject: Replacement Text Date: 01/07/2015 12:12:29
is

Number: 34 Author: djw Subject: Cross-Out Date: 01/07/2015 12:16:04

Number: 35 Author: djw Subject: Sticky Note Date: 01/07/2015 12:16:40
Repeat of 'optimizations'.

Number: 36 Author: djw Subject: Sticky Note Date: 01/07/2015 12:17:46
Sentences 2 and 3 here really say nothing new.

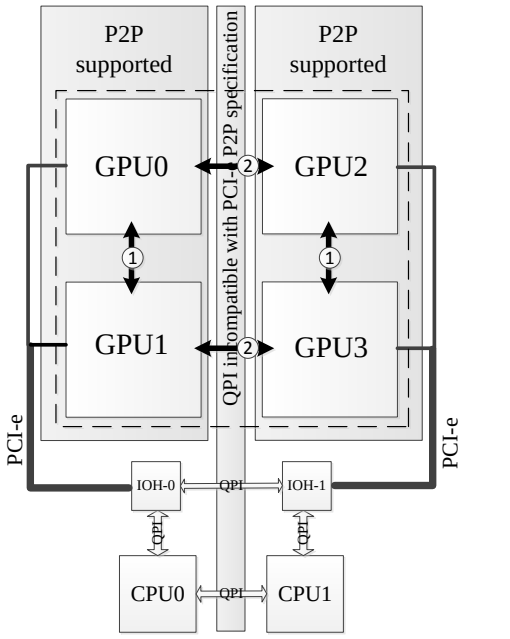

Figure 5. Communications pattern among multiple GPUs in one node

Second, we take full consideration of the architecture of our platform in which 4 GPUs are connected with two I/O Hubs (IOHs). As illustrated in Fig. 5, there are two Intel SandyBridge CPUs that connect two GPUs. Both the CPUs are themselves connected through Intel QuickPath Interconnect (QPI). Notation ① means that the communications between GPUs are connected with the same IOH support Peer-to-Peer (P2P) access. Notation ② represents the communications in which P2P access is not supported. If MPI_Rank 0 (context on GPU-0) sends data to MPI_Rank 2 (context on GPU-2), rank 0 must switch its context to GPU-2 temporally and opens the corresponding memory handles to obtain the device buffer pointers of rank 2. For ~~those~~ that do not support P2P ~~access between one another,~~ we must switch context to the same GPU before opening the corresponding memory handles. We then call ~~regular~~ $cudaMemcpyAs$ nctions to ~~fulfill~~ ata ~~ommunications. For communications between GPUs on the same IOH, the switching context is not necessary.~~ Although the function cudaMemcpyAsync is used in the communication of both ① and ②, the NVVP software shows that ① does a device-to-device memory copy that bypasses the CPU, whereas ② does a device-to-host and a host-to-device memory copy that involves the CPU. The 2-D decomposition introduced in Fig. 5 is an example to demonstrate our design can easily extend to 8 or more GPUs within one node.

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Number: 1 Author: djw Subject: Sticky Note Date: 01/07/2015 12:27:17
Explain what you mean by a context.

First you seem to imply that a MPI process running on one CPU starts using the second CPU memory.

Later you imply that you mean the GPUs themselves start changing the CPUs that are connected with.

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Number: 3 Author: djw Subject: Sticky Note Date: 01/07/2015 12:28:33
Should this be the same CPU?

Number: 4 Author: djw Subject: Replacement Text Date: 01/07/2015 12:27:45
pairs of

Number: 5 Author: djw Subject: Cross-Out Date: 01/07/2015 12:30:13

Number: 6 Author: djw Subject: Cross-Out Date: 01/07/2015 12:28:55

Number: 7 Author: djw Subject: Sticky Note Date: 01/07/2015 12:29:36
Where has an IOH been defined?

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send the

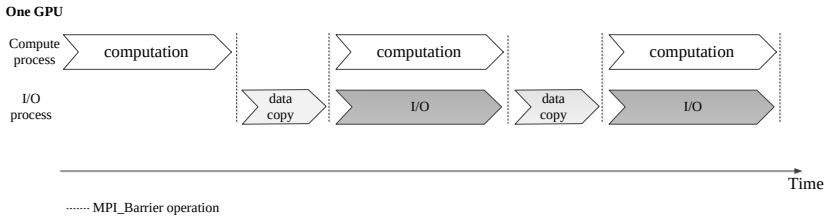

Figure 6. One computing process and one I/O process both set their contexts on the same GPU. During the data copy phase, the computing process remains idle and the I/O process will copy data from the GPU to the CPU host through the $cudaMemcpy$ function.

4.3 I/O optimizations between hybrid GPU and CPU

The time consumed for I/O in the original mpiPOM is not significant because the output frequency is relatively low. However, after we fully accelerate the model by GPU, the I/O overhead, which is approximately 30% of the total runtime, cannot be ignored. As described in Sec. 4.2, each MPI process sets its context on one GPU and is responsible for la[1]g kernel functions on this GPU, and the CPU is used to collect and output data. In fact, in most climate models, includin[2]mpiPOM, the computing phase and I/O phase run alternately. In a sense, the computing phase and the I/O phase are serial, which means that the GPU will remain idle until the CPU finishes I/O operations. Huang et al. (2014) designed a fast I/O library for climate models and provided automatic overlapping of I/O and computing. Motivated by their work, we design a method so that computations on GPU and I/O operations on CPU can run in parallel.

Because MPI processes are blocked during the output phase and cannot launch kernels to GPUs, we choose to launch more MPI processes. We divide all the MPI processes into computing processes and I/O processes with different MPI communicators. The computing processes are responsible for launching kernel functions as usual, and the I/O processes are responsible for output. One I/O process attaches to one computing process and these two processes set their contexts on one single GPU through $cudaSetDevice$ function.[3] ~~The total number of MPI processes are twice the size they were before.~~

Since the I/O processes must fetch data from the GPU,[4] ~~where the data are allocated by the computing processes,~~ communication is necessary between them.[5] ~~Here, we again utilize the feature of CUDA IPC, as introduced in Sec. 4.2.~~ [6]~~Through CUDA~~ IPC, the I/O processes obtain the device buffer pointers from the computing processes during the initialization phase. When there is a need to output data, the computing processes are blocked and kept idle for a short time while waiting for[7] I/O processes to fetch data. Then, the computing processes continue their computation, and the I/O processes complete their output in the background, as illustrated in Fig. 6.

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Number: 1 Author: djw Subject: Sticky Note Date: 01/07/2015 12:37:25

1. I am not sure 'most' is correct.

2. POM is not a climate model.

3. Many PVM and MPI codes, including moma/OCCAM were using multi-processors to overlap CPU and I/O 20 years ago

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This repeats the previous sentence.

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Number: 4 Author: djw Subject: Cross-Out Date: 01/07/2015 12:39:19

Number: 5 Author: djw Subject: Cross-Out Date: 01/07/2015 12:39:37

Number: 6 Author: djw Subject: Replacement Text Date: 01/07/2015 12:39:57

Using

Number: 7 Author: djw Subject: Sticky Note Date: 01/07/2015 12:43:45

Why did not not place the archive data into a set-aside buffer and carry on with the main calculation. The I/O processes on the CPU then copies across the set-aside data without on the fly.

The advantage of this method is that it overlaps the I/O on the CPU with computation on the GPU. In the serial I/O, the computing processes are blocked while data are brought to the host and written to disk. In the overlapping I/O, the computing processes wait for the data to be brought to the host. In addition, the bandwidth of data brought to the host through the PCI express bus is approximately 6 GBps, but the output bandwidth is approximately 100 MBps, as determined by the disk. Therefore, the overlapping method significantly accelerates the entire application.

Note that there are more than 50 kernel functions in the current version of gpuPOM. The main reason that we have a large number of kernels in gpuPOM is that there exist numerous subroutines in mpiPOM. Since we port the entire model one subroutine by one subroutine, which is a convenient way to debug the gpuPOM and to guarantee its bit by bit identical results to mpiPOM, we need to write a large number of GPU kernels. Further more, we break several subroutines of mpiPOM into several GPU kernels of gpuPOM in 3 cases: when subroutine B is invoked in subroutine A(illustrated in Fig. 7(a)), when a MPI function call is invoked in subroutine A(illustrated in Fig. 7(b)), and when interior array is first written by one thread and later read by adjacent threads, in the mean while caching this array in shared memory makes no sense(illustrated in Fig. 7(c)). Although function fusion has been done as described in Section 4.1 (**D**), aggressive function fusion to make use of data locality between functions is a promising optimization(Wahib and Maruyama, 2014). But, a redesign of the code structure of mpiPOM is needed and it is a part of our future work.

5 Experiments

In this section, we first describe the specification of our platform and comparison methods used to validate the correctness of the gpuPOM. Furthermore, we present the performance and scalability of the gpuPOM on the GPU platform in comparison with the mpiPOM on the CPU platform.

5.1 Platform Setup

The GPU platform used in our experiments is a super workstation computer consisting of two CPUs and 4 GPUs, as illustrated in Fig. 5. The CPUs are 2.6 GHz 8-core Intel E5-2670 (architecture code-named SandyBridge), which can turbo to 3.0 GHz when all 8 cores are utilized. The peak single-precision performance of the Intel SandyBridge CPU is 384 GFlops and the peak memory bandwidth is 51.2 GBps. The GPUs are Nvidia Telsa K20X, equipped with 2,688 GPU-cores and 6 GB GDDR5 fast on-board memory. The peak single-precision performance of K20X GPU is 3.95 TFlops and the peak memory bandwidth is 250 GBps. Therefore, the aggregated performance provided with 4 GPUs can reach 16 TFlops and 1 TBps memory bandwidth, which is sufficient to execute the general simulation research for regional ocean models thus far. The operating system is RedHat Enterprise Linux 6.3 x86_64. The programs on this platform are complied with Intel compiler v14.0.1, Intel MPI Library v4.1.3 and CUDA 5.5 Toolkit. For the purposes of comparison, the CPU platform used

Page: 17

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It overlaps the CPI to disk I/O with the calcualtion but not the GPU to CPU communication.

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Number: 3 Author: djw Subject: Inserted Text Date: 01/07/2015 12:46:16
GPU

Number: 4 Author: djw Subject: Replacement Text Date: 01/07/2015 12:46:07
sent

Number: 5 Author: djw Subject: Cross-Out Date: 01/07/2015 12:46:33

Number: 6 Author: djw Subject: Inserted Text Date: 01/07/2015 12:46:51
only

Number: 7 Author: djw Subject: Replacement Text Date: 01/07/2015 12:46:55
sent

Number: 8 Author: djw Subject: Cross-Out Date: 01/07/2015 12:47:21

Number: 9 Author: djw Subject: Inserted Text Date: 01/07/2015 12:47:30
to disk

Number: 10 Author: djw Subject: Inserted Text Date: 01/07/2015 12:47:47
speed of the

Number: 11 Author: djw Subject: Replacement Text Date: 01/07/2015 12:48:45
is that

Number: 12 Author: djw Subject: Cross-Out Date: 01/07/2015 12:48:48

Number: 13 Author: djw Subject: Replacement Text Date: 01/07/2015 12:49:15
at a time.

Number: 14 Author: djw Subject: Replacement Text Date: 01/07/2015 12:51:20
This was done to simplify debugging of

Number: 15 Author: djw Subject: Cross-Out Date: 01/07/2015 12:51:45

Number: 16 Author: djw Subject: Cross-Out Date: 01/07/2015 12:51:35

Number: 17 Author: djw Subject: Replacement Text Date: 01/07/2015 12:51:56
Furthermore

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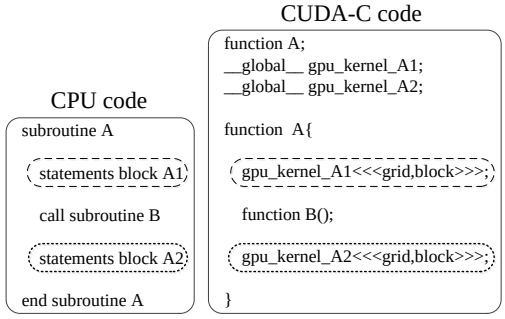
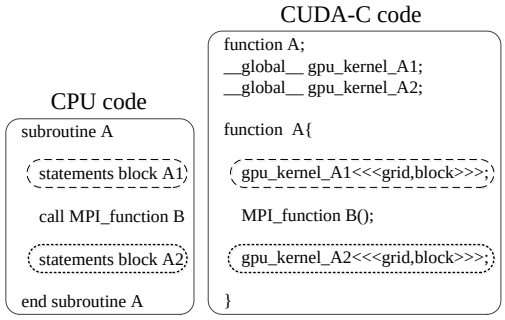
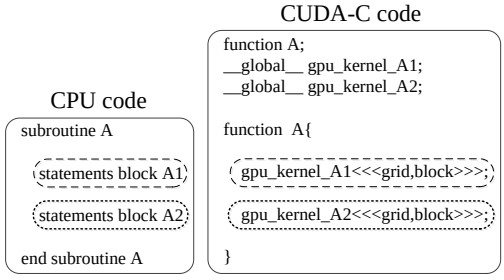
in the three cases where



(a)when subroutine B is invoked in subroutine A, A is broken into 2 small kernels.



(b)when a MPI function call is invoked in subroutine A, A is broken into 2 small kernels.



(c)when interior array is first written by one thread and later read by adjacent threads, in the mean while caching this array in shared memory makes no sense, A is broken into 2 small kernels.

Figure 7. The 3 cases when a subroutine is broken into small kernels.

in our experiments is the $Tansuo100$ supercomputer at Tsinghua University, which consists of 740 nodes, each of which has two 2.93 GHz 6-core Intel Xeon X5670 processors and 32 GB memory. The nodes are connected through an Infiniband network, which provides a maximum bandwidth of 40 Gbps. The node operating system is RedHat Enterprise Linux 5.5 x86_64. All the programs on this platform are compiled with Intel compiler v11.1, and the MPI environment is Intel MPI v4.0.2.

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The Original mpiPOM code is benchmarked with its initial compiler flags(i.e., -O3 -precise) and also with the same Intel compiler. We also use the GPUDirect technology within MVAPICH2 v1.9 to test the communication effects among multiple GPUs, and compare the results with our implementation.

5.2 The test case and the verification of accuracy

The "dam break" simulation (Oey, 2014) is conducted to verify the correctness and test the performance and the scalability of the gpuPOM. It is a baroclinic instability problem which simulates flows produced by horizontal temperature gradients. The model domain is configured as a straight channel with uniform depth of 50 m. Periodic boundary conditions are used in the east-west direction, and the channel is closed in the north and south. Its horizontal resolution is $1km \times 1km$. To test large computational grid, the domain size of this test case is increased to 962×722 horizontal grid points and 51 vertical sigma levels, which is limited by the capacity of on-board memory. Initially, temperature in the southern half of the channel is 15^oC and 25^oC in the northern half. The salinity is fixed at 35 psu. The fluid is then allowed to adjust. In the first 3-5 days, geostrophic adjustments occurs. Then unstable wave develops due to baroclinic instability. Eventually, eddies are generated. Figure 8 shows the sea-surface height (SSH), sea-surface temperature (SST), and currents after 39 days. The development of a gravity wave is manifest. Noticeably, The gravity wave is confined in the middle of the channel by Rossby radius deformation.

To verify accuracy, we check the binary output files output from the original mpiPOM and the gpuPOM. This testing method is also used in the GPU-porting of ROMs (Mak et al., 2011). As introduced in Whitehead and Fit-Florea (2011), the same inputs will give identical results for individual IEEE-754 operations except in a few special cases. These cases can be classified into three categories: different operations orders, different instructions and different implementations of math libraries. For the first in our study, the parallelization of the mpiPOM does not change the order of each floating point operation and we benefit from this. For the second case in our study, the GPUs have fused multiply-add (FMA) instruction while the CPU does not in our CPU platform. Because this instruction might cause a difference in the numerical results, we disable FMA instructions with the "-fmad=false" compiler flag for the GPUs. For the third case in our study, the value of exponent used in the GPU has a maximum of 2 rounding errors NVIDIA (2014). Fortunately, in the execution path of our dam break simulation, the power of the exponent functions remains unchanged over the entire simulation. Therefore, we accomplish this function on the CPU during the initialization phase and copy the results to the GPU for later data reuse. The experimental results demonstrate that the output variables regarding velocity, temperature, salinity and sea surface height are identical.

5.3 Performance

To understand the advantages of the optimizing methods introduced in Sec. 4, we test the dam break case with different experiments . The current dam break case uses single-precision format. The

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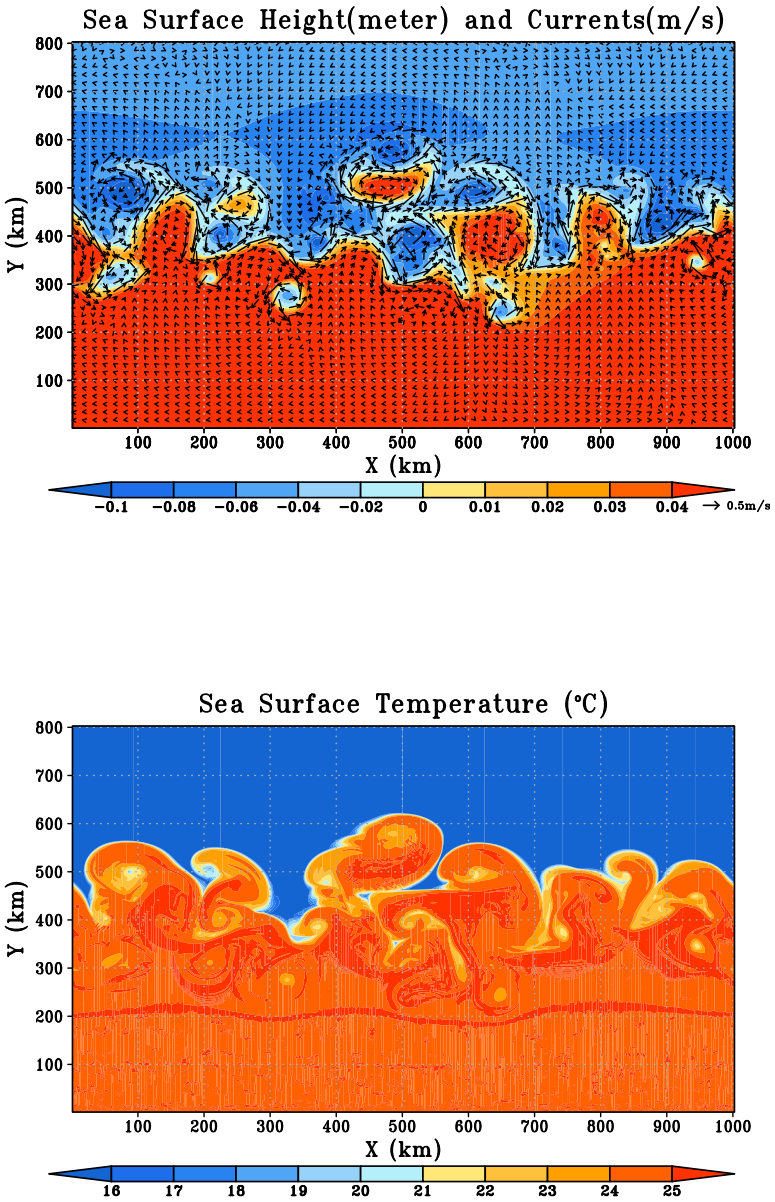

Figure 8. The model results after 39 days simulation. For the up figure, color shading is the Sea Surface Height (SSH). Vectors are ocean current. For the low figure, color shading is the Sea Surface Temperature (SST). Several warm and cold eddies are generated in the middle of the domain where SST gradient is largest. Noticeably, the gravity wave is confined in the middle of the channel by Rossby radius deformation.

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metrics of seconds per simulation day, which is the walltime it requires to obtain 24 hours in the simulation, is measured and used to compare the performance.

In the first experiment, we compare the gpuPOM with the mpiPOM on different hardware platforms, including K20X GPU, the Intel Westmere 6-cores X5670 CPU and the Intel SandyBridge E5-2670 CPU. Fig. 9 shows that one K20X GPU can compete with approximately 55 Intel SandyBridge CPU cores or 95 Intel Westmere CPU cores. Obtaining such a speedup on a pure CPU platform is reasonable. Taking the SandyBridge CPU platform as an example, the theoretical memory bandwidth of one 8-core E5-2670 CPU is 51.2 GBps, and the peak single-precision floating point performance is 384 GFlops with all 8 cores turbo to 3.0 GHz. However, for K20X GPU, the memory bandwidth and peak single-precision floating point performance are 250 GBps and 3.95 TFlops, respectively. The approximate ratio of memory bandwidth between one SandyBridge CPU and one K20X GPU is $1:5$, and the ratio of floating points performance between one SandyBridge CPU and one K20X GPU is $1:10$. Namely, if an application is strictly memory bound, one K20X GPU can compete with 5 SandyBridge CPUs. In addition, if an application is strictly computing bound, it can compete with 10 SandyBridge CPUs. As the mpiPOM is memory bound, according to the memory bandwidth ratio between the CPU and the GPU, our gpuPOM should provide equivalent performance to 5x8 = 40 CPU cores. Combining our careful memory optimizations, our final design achieves another performance boost of 25%, and one GPU provides similar performance to more than 50 Intel 8-core SandyBridge CPU cores. Compared with Intel Westmere 6-cores CPU, our results provide similar performance to more than 95 CPU cores.

The performance API tool (PAPI) shows that the performance of the gpuPOM on single K20X is 107.3Gflops in single-precision for the 962*722*51 grid size. The low performance in Gflops reflects the memory-bound problem in climate models. Previous work such as time skewing (McCalpin and Wonnacott (1999); Wonnacott (2000)) can make a stencil computation compute bound by making use of data locality between different time-steps. However, for real-world climate models including mpiPOM, the code is usually tens to hundreds of thousands lines and analyzing the dependency manually is tough. Designing an automated tool to further analyze and optimize the mpiPOM and the gpuPOM is a part of our future work.

In the second experiment, we test the communication overlapping method used in the gpuPOM and compare it with the MVAPICH2. In the current MVAPICH2, the communication and boundary operations are not overlapping with computing. Fig. 10 shows the weak scaling performance of the gpuPOM on multiple GPUs. To maximize performance, the grid size for each GPU is set to $962 \times 722 \times 51$. When using 4 GPUs with the implementation of MVAPICH2, 18% of the total runtime is consumed in executing the communication and boundary operations. This overhead does not exist in our communication overlapping method. Fig. 10 shows that it spends almost the same time when using different GPUs because the communication and boundary operations are almost fully overlapped with the inner part of the computation.

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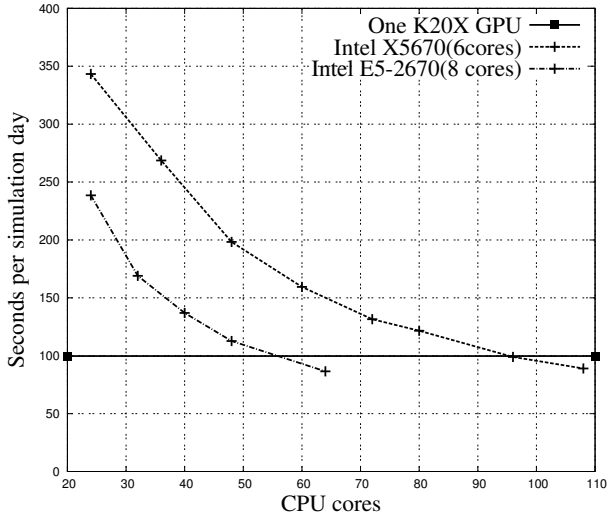

Figure 9. Performance comparison with different hardware platform

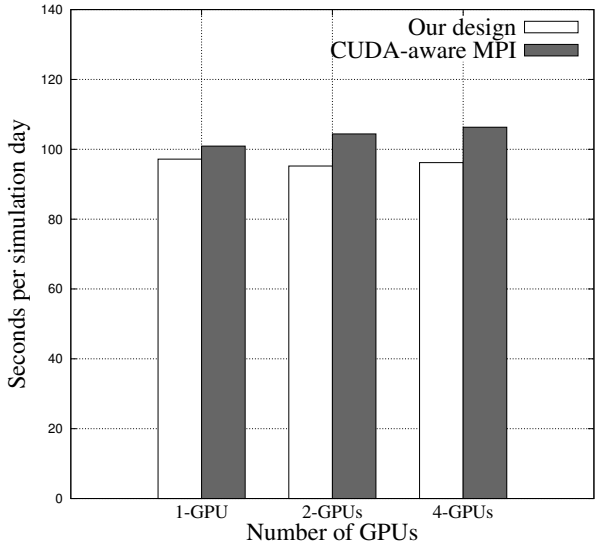

Figure 10. The weak scaling test between our communication overlapping method and the MVAPICH2 subroutines.

In the third experiment, we test the efficiency of the gpuPOM on multiple GPUs. Table 2 shows the strong scaling result of the gpuPOM on multiple GPUs. We fix the global grid size at $962 \times 722 \times 51$ and increase the amount of GPUs gradually. The results show that the strong scaling efficiency is 99% on 2 GPUs and 92% on 4 GPUs. A smaller subdomain will decrease the performance of the gpuPOM in two aspects. First, communication time can easily exceed the computation time in the inner part and cannot be overlapped. As the subdomain size decreases, the inner part computation

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time decreases, but the communication time will not decrease because latency is the dominant factor. Second, the latency of kernel launching and overhead of implicit synchronization after kernel execution will not decrease. There are a series of small kernels in the gpuPOM, and the execution time is close to launching latency and synchronization overhead. When the subdomain size decreases, the impact of these delays expands.

Table 2. The strong scaling result of gpuPOM

Number of GPUs	1-GPU	2-GPUs	4-GPUs
Time(s)	97.2	48.7	26.3
Efficiency	1.00	0.99	0.92

In the fourth experiment, we test the performance of the I/O overlapping method and compare it with the default parallel NetCDF (PnetCDF) method and NO-I/O method. NO-I/O means that all I/O operations are disabled in the program and the time measured is the pure computing time. We simulated the experiment for 20 days and output the history files daily in the netCDF format. The variables included in the output netCDF files are 2-dimensional arrays of size 722×482 and 3-dimensional arrays of size $722 \times 482 \times 51$. The final history files are approximately 12 GB. Fig. 11 shows that the I/O overlapping method outperforms the default PnetCDF method. For 1 GPU and 2 GPUs, the overall runtime decreases from1694/1142 seconds to 1239/688 seconds, which is close to the NO-I/O method. The small difference between our design and NO-I/O is that the computing processes must be blocked until I/O processes bring data from the GPU. For the case of 4 GPUs, the output time is longer than computational time because the latter is fast and the I/O time is relatively large such that the I/O phase cannot fully overlap with the computing phase. The overall runtime equals the sum of the computation time and the non-overlapped I/O time.

In the last experiment, we test different workloads with the gpuPOM and compare the results with the mpiPOM on $Tansuo100$ platform. The available global grid size are choosen from the three different high-resolution sets (Grid-1: $962 \times 722 \times 51$, Grid-2: $1922 \times 722 \times 51$, Grid-3: $1922 \times 1442 \times 51$). Fig. 12 shows that our workstation with 4 GPUs is comparable to a powerful cluster with 408 CPU cores (34 nodes * 12 cores/node) for the simulation of mpiPOM. Since the Thermal Design Power(TDP) of one X5670 CPU(6-cores) is 95W and that of one K20X GPU is 235W, it means using 4 GPUs brings 6.8 times less energy consumption compared with 408 CPU cores. Small subdomains will decrease the performance of the gpuPOM as discussed in the strong scaling test, but it may greatly benefit the mpiPOM on the CPU. The last level cache of one SandyBridge CPU in our platform is 20 MB, whereas that of K20X GPU is only 1.5 MB. As the subdomain size for each MPI process decreases, the cache hit ratio will increase on a pure CPU platform, which can surely improve the performance especially for the memory-bound problem. However, for the simulation on 408 CPU cores, the MPI communication time may occupy more than 40% of total execution time.

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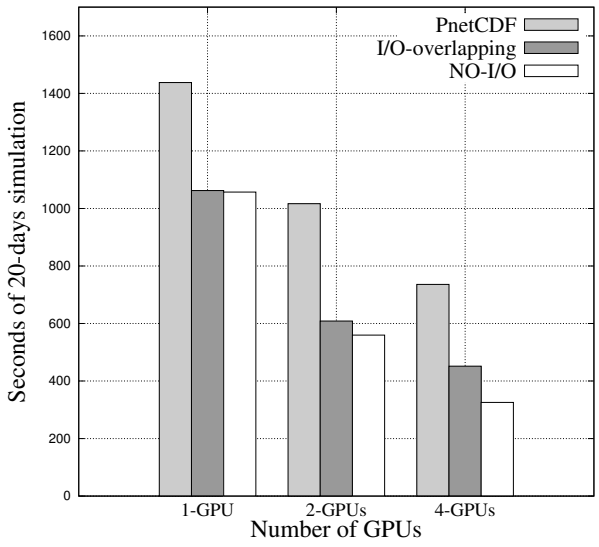

Figure 11. I/O Test for gpuPOM

With the number of cores increasing to over 450, the execution time may increase instead, as shown in Fig. 12. As a result, our GPU solution has an overwhelming advantage compared to the CPU because the communication overhead is less expensive and overlapped.

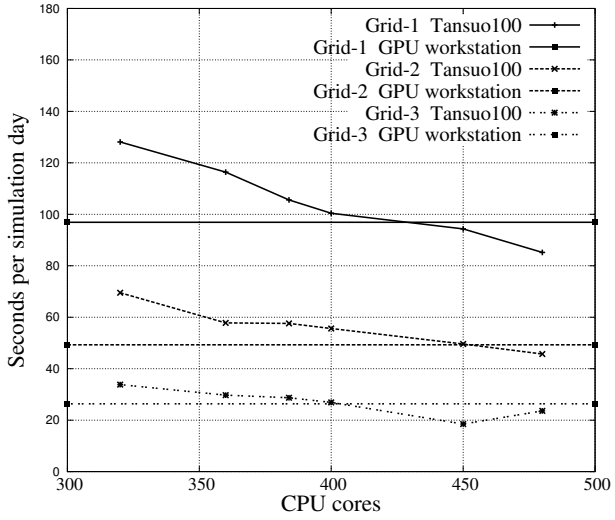

Figure 12. Four GPUs performance test compared with $Tansuo100$ clusters(Intel Westmere CPUs)

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6 Code availablity

The gpuPOM used to simulate the regional ocean dynamic and physical process releases with the version 1.0 series, which is freely available at https://github.com/hxmhuang/gpuPOM. Note that the testing script "run_exp002.sh" can be downloaded to compile and execute the codes, and to reproduce the test case.

7 Conclusions

In this paper, we provide a full GPU accelerated solution of POM. Unlike partial GPU porting, such as WRF and ROMs, the gpuPOM does all the computations on the GPU. The main contribution of our work includes a better use of state-of-the-art GPU architecture, particularly regarding the memory subsystem, a new design of a communication and boundary operations overlapping approach and a new design of an I/O overlapping approach. With the workstation with 4 GPUs, we achieve over 400x speedup against a single CPU core, and provide equivalent performance to a powerful CPU cluster with more than 400 cores and reduce the energy consumption by 6.8 times. This work provides cost-effective and efficient ways in ocean modeling.

Acknowledgements. This work is supported in part by a grant from the Natural Science Foundation of China(41375102), the National Grand Fundamental Research 973 Program of China (No. 2014CB347800), and the National High Technology Development Program of China (2011AA01A203).

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